AXS2050

PSRR

PLL 300kHz 1.2MHz
AM

AXS2050 HTSSOP32

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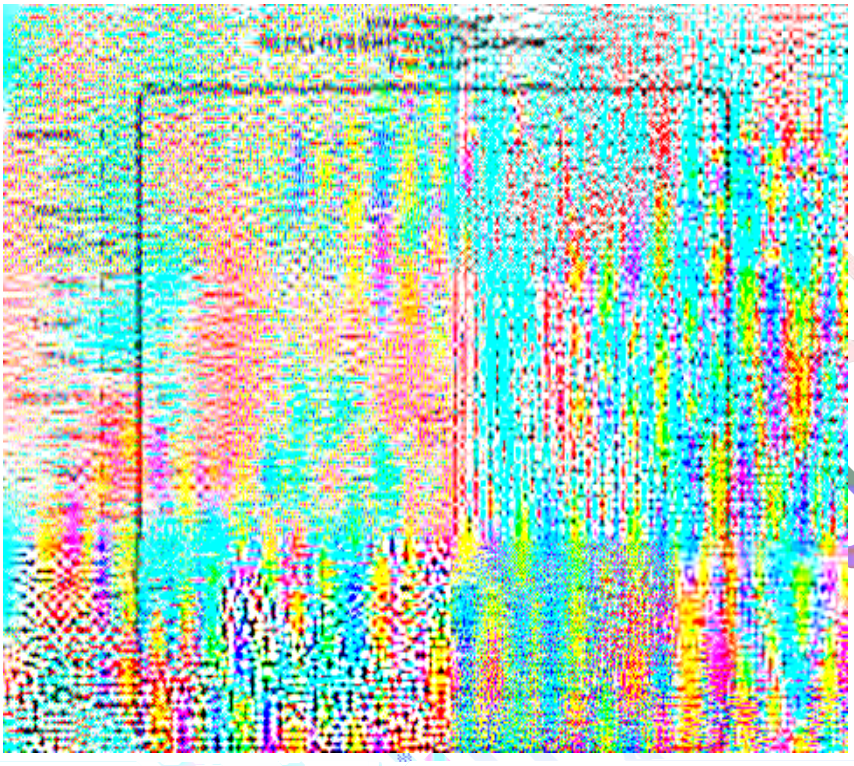
- ■ D

  BTL 2x50W 4Ω 10% THD+N 21V
  BTL 2x75W 4Ω 10% THD+N 24V
  PBTL 1x100W 2Ω 10% THD+N 21V
  PBTL 1x145W 2Ω 10% THD+N 24V
- ■ POP
- ■ >90%
- ■ 12mA @12V
- ■
- ■
- ■
- ■ KTV

Pin Configuration and Functions



PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	MODSEL	I	Internal fixed BD mode. No Connect Pin. Can be shorted to PVCC or shorted to GND or left open.
2	SDZ	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC. Refer to: Startup and Shutdown Operation
3	FAULTZ	DO	General fault reporting including Over-temp, DC Detect. Open drain. Refer to: Device Protection System FAULTZ = High, normal operation FAULTZ = Low (an external 100 k pull-up resistor required), fault condition
4	RINP	I	Positive audio input for right channel. Connect to GND for MONO mode.
5	RINN	I	Negative audio input for right channel. Connect to GND for MONO mode.
6	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit. Refer to: PLIMIT Operation
7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the PLIMIT and GAIN/SLV resistor dividers. Refer to: GVDD Supply
8	GAIN/SLV	I	Selects Gain and selects between Master and Slave mode depending on pin voltage divider. Refer to: Gain Setting and Master and Slave
9, 25	GND	G	Ground
10	LINP	I	Positive audio input for left channel. Connect to GND for PBTL mode.
11	LINN	I	Negative audio input for left channel. Connect to GND for PBTL mode.
12	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	AM2	I	AM Avoidance Frequency Selection
14	AM1	I	AM Avoidance Frequency Selection
15	AM0	I	AM Avoidance Frequency Selection
16	SYNC	DIO	Clock input/output for synchronizing multiple Class-D devices. Direction determined by GAIN/SLV terminal. Refer to: Gain Setting and Master and Slave
17	AVCC	P	Analog Supply
18,19	PVCC	P	Power supply

20	BSNL	BST	Boot strap for negative left channel output, connect to 220 nF X5R, or better ceramic cap to OUTPL
21	OUTNL	PO	Negative left channel output
23	OUTPL	PO	Positive left channel output
24	BSPL	BST	Boot strap for positive left channel output, connect to 220 nF X5R, or better ceramic cap to OUTNL Refer to: BSPx and BSNx Capacitors
22, 28	GND	G	Ground
26	BSNR	BST	Boot strap for negative right channel output, connect to 220 nF X5R, or better ceramic cap to OUTNR. Refer to: BSPx and BSNx Capacitors
27	OUTNR	PO	Negative right channel output
29	OUTPR	PO	Positive right channel output
30	BSPR	BST	Boot strap for positive right channel output, connect to 220 nF X5R or better ceramic cap to OUTPR. Refer to: BSPx and BSNx Capacitors
31, 32	PVCC	P	Power supply
		G	Connect to GND for best system performance. If not connected to GND, leave floating.

Order Information

Part Number	Package Type	Marking	Package Qty	Temp Range (°C)

Specifications

1. Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	0.3	30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	0.3	6.3	V
	PLIMIT, GAIN/SLV, SYNC	0.3	GVDD+0.3	V
	AM0, AM1, AM2, MUTE, SDZ, MODSEL	0.3	PVCC+0.3	V
Slew rate, maximum(2)	AM0, AM1, AM2, MUTE, SDZ, MODSEL		10	V/ms
Operating free-air temperature, T_A		40	125	°C
Operating junction temperature , T_J		40	150	°C
Storage temperature, T_{stg}		40	125	°C
Lead Temperature (Soldering, 10s)			260	°C

(1)

(2)

2. ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM)	±2000	V
	Charged-device model (CDM)	±500	

3. Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}	5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL	2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 k , PV_{CC} = 26 V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ, MODSEL (V_I = 2 V, V_{CC} = 18 V)			50	µA
R_L(BTL)	Minimum load Impedance	Output filter: L = 10 µH, C = 680 nF	3.2	4		
R_L(PBTL)		Output filter: L = 10 µH, C = 1 µF	1.6	2		
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition	1			µH

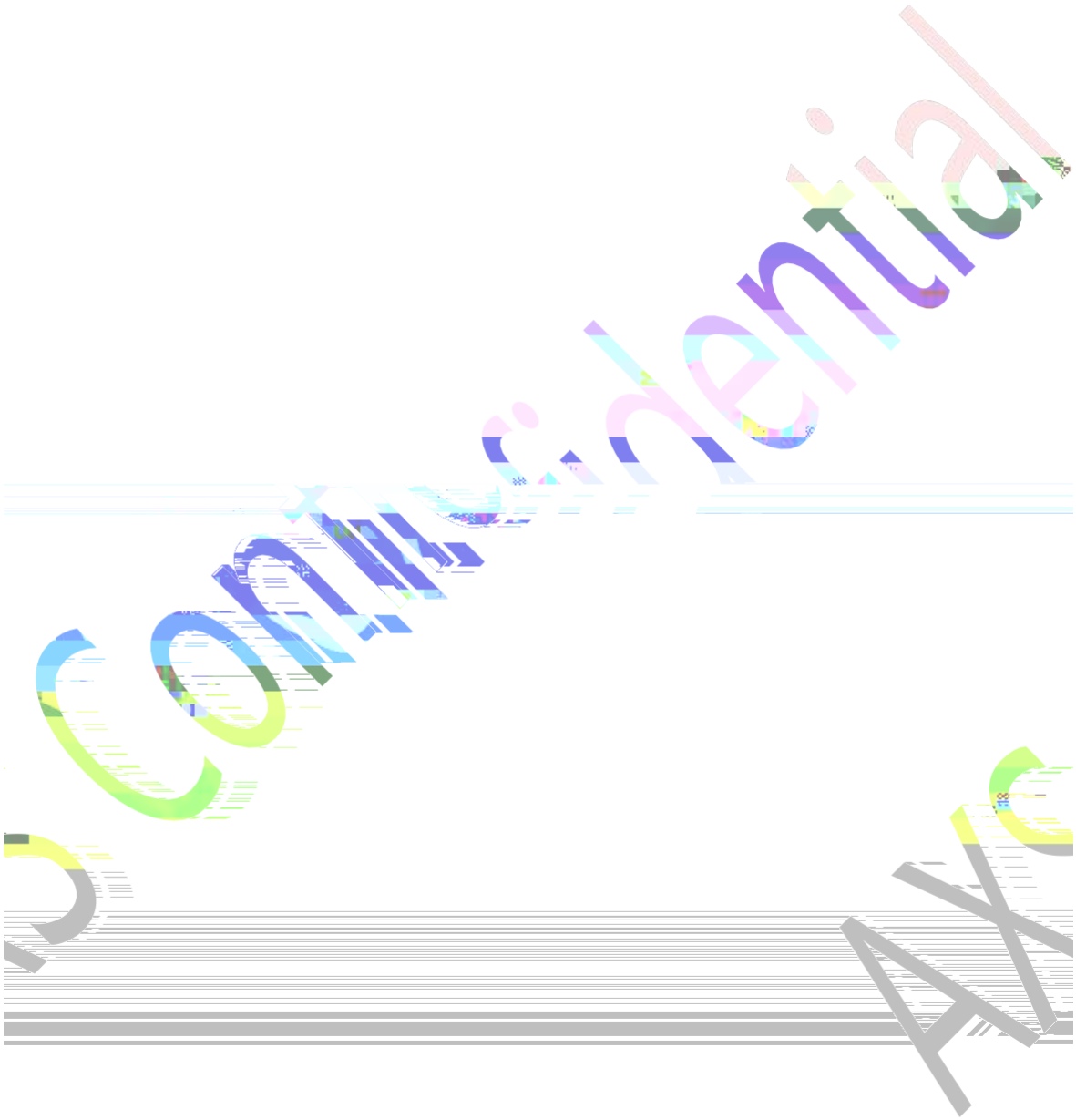
4. Thermal Information

THERMAL METRIC		AXS2050 DAD(1) 32 PINS	UNIT
R_{JA}	Junction-to-ambient thermal resistance	N/A	°C/W
$R_{JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
$_{JT}$	Junction-to-top characterization parameter	1.2	°C/W
$_{JB}$	Junction-to-board characterization parameter	21	°C/W

5. DC Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V		1.5	5	mV
I_{CC}	Quiescent supply current	SDZ = 2 V, With load and filter, PV_{CC} = 12 V		12		mA
		SDZ = 2 V, With load and filter, PV_{CC} = 24 V		17		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ = 0.8 V, With load and filter, PV_{CC} = 12 V		20		µA
		SDZ = 0.8 V, With load and filter, PV_{CC} = 24 V		30		
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PV_{CC} = 21 V, I_{out} = 500 mA, T_J = 25°C		90		m
		R1 = 5.6 k				

7. Typical Characteristics



Typical Characteristics (continued)

Typical Characteristics (continued)

Typical Characteristics (continued)

3. Feature Description

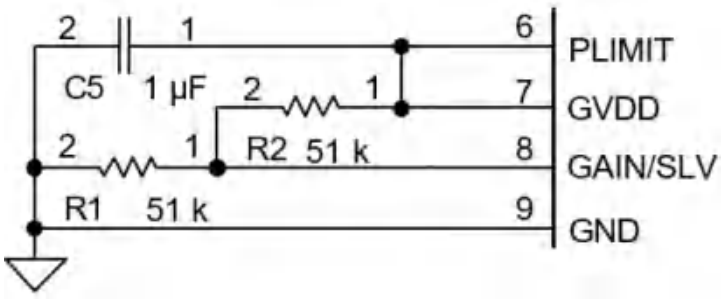
3.1 Gain Setting and Master and Slave

The gain of the AXS2050 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four states set the GAIN in Master mode with gains of 20, 26, 32, and 36 dB respectively, while the next four states set the GAIN in Slave mode with gains of 20, 26, 32, and 36 dB respectively. The gain setting is latched during power- up and cannot be changed while the device is powered on.

1 lists the recommended resistor values for different state settings.

1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 k	OPEN	60 k
Master	26 dB	20 k	100 k	30 k
Master	32 dB	39 k	100 k	15 k
Master	36 dB	47 k	75 k	9 k
Slave	20 dB	51 k	51 k	60 k
Slave	26 dB	75 k	47 k	30 k
Slave	32 dB	100 k	39 k	15 k
Slave	36 dB	100 k	16 k	9 k



25. Gain, Master/Slave

In Master mode, the SYNC terminal is an output, while in Slave mode, the SYNC terminal is an input for a clock. TTL logic levels with compliance to GVDD.

3.2 Input Impedance

The AXS2050 input stage is a fully differential input stage and the input impedance changes with the gain 1 lists the values from min to max gain. The tolerance

inputs must be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF.

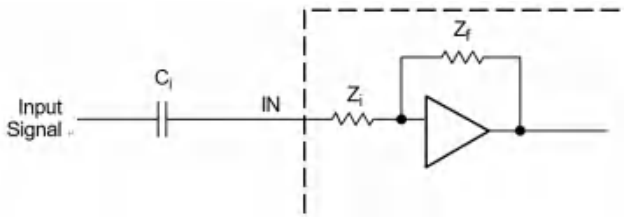
The input AC-coupling capacitor along with the input impedance forms a high-pass filter with the following cut-off frequency:

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz.

2 lists the recommended AC-coupling capacitors for each gain setting. If a 3-dB frequency response is accepted at 20 Hz, 10 times lower capacitors (for example, a 1-µF capacitor) can be used.

2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	50 k	1.5 µF	2.1 Hz
26 dB	25 k	3.3 µF	1.9 Hz
32 dB	12.5 k	5.6 µF	2.3 Hz
36 dB	7.3 k	10 µF	2.2 Hz



26. Input Impedance

The input capacitors should be a type of low leakage, such as quality electrolytic, tantalum, or ceramic caacitors.

If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

3.3 Startup and Shutdown Operation

The AXS2050 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low puts the outputs to mute and the amplifier to enter a low-current state. Do not leave SDZ unconnected, because the amplifier operation is unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle, and cannot be changed until the next power- up.

3.4 PLIMIT Operation

The AXS2050 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail. The amplifier operates as if it was powered by a lower supply voltage, and thereby, limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1-µF capacitor

27. Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This is done by limiting the duty cycle to a fixed maximum value. The limit can be considered as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately four times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$ for unclipped power

where

P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

R_L is the load resistance.

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.

V_P is the peak amplitude, which is limited by

3.6 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input. (See the application circuit diagram in 32.) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

3.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the AXS2050 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input.

To use the AXS2050 with a single-ended source, AC ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be AC grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible to allow the input DC blocking capacitors to become completely charged during the 40-ms power-up time. If the input capacitors are not allowed to completely charged, there will be some additional sensitivity to the component matching which can result in pop if the input components are not well matched.

3.8 Device Protection System

The AXS2050 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the ent . m0 gT/F2 9.96 Tf1 0 0 1 138.5 695.62 Tm0 g0 G[m)-21(us)-3(t)474.22 Tf1 96 Tf7.68 4

4. Device Modulation Scheme

The AXS2050 is internally fixed to BD mode for better performance.
This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires.
Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker.
The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages.
The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

28. BD Mode Modulation

5. Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

Many traditional Class-D amplifiers are based on the AD modulation. Due to the out-of-phase nature of a BTL or PBTL amplifier operating in the AD modulation, if no LC filter was present, the load sees the full PWM signal across its terminals. This causes a high-frequency ripple current to pass through the load, which leads to high power dissipation, poor efficiency, and potential speaker damage. The ripple current is large in the AD modulation scheme, because it is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × VCC, and the time at each voltage is half the period for the AD modulation scheme. An ideal LC filter is required to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The modulation schemes implemented in the AXS2050 have little loss in the load even without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases and the pulses widen, the ripple current can go up. In this case, the ripple current can be filtered with an LC filter for increased efficiency. However, in most applications the filter is not required.

With an LC filter, specifically as the cut-off frequency of the LC filter is smaller than the PWM switching frequency of the amplifier, the ripple current is reduced such that only a small residual ripple voltage is present after the LC filter. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, hence increasing efficiency.

6. Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the AXS2050, a high efficiency Class-D audio amplifier can be designed while minimizing interference to the surrounding circuits. Designing the amplifier can also be accomplished with only a low-cost ferrite bead filter. In this case the user must carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, therefore the user must select a material that is effective in the 10-MHz to 100-MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30-MHz. The ferrite bead filter should be used to block radiation in the 30-MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000-pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead or capacitor filter should be less than 10-MHz.

Also, the ferrite bead must be large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, the device can also estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. A high quality ceramic capacitor is also required for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the Class-D outputs to ground. Suggested values for a simple RC series snubber network would be 18- in series with a 330-pF capacitor, although design of the snubber network is specific to different applications and must be designed with the consideration of the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, verify the layout of the snubber network is tight and returns directly to the GND pins on the IC.

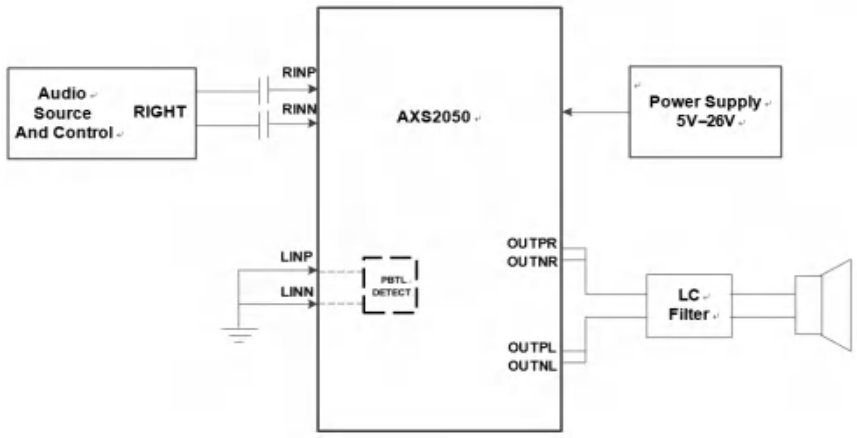
9.1 Mono PBTL Mode

In mono PBTL mode, the device can deliver up to 100-W output power. Configuration steps for mono PBTL mode are as follows:

Connect LINP and LINN directly to Ground (without capacitors), so the device is set in a mono PBTL mode during power up.

Connect OUTPR and OUTNR together for the positive speaker terminal, and OUTNL and OUTPL together for the negative speaker terminal.

- Analog input signal is applied to RINP and RINN.



30. Mono PBTL Mode

9.2 Mono BTL Mode (Single Channel Mode)

The AXS2050 can be connected in mono BTL mode while cutting the idle power-loss nearly by half.

- Connect RINP and RINN directly to Ground (without capacitors), so the device is set in mono BTL mode during power up.
- Connect OUTPL to the positive speaker terminal, and OUTNL to the negative speaker terminal.
- Analog input signal is applied to LINP and LINN.

31. Mono BTL Mode

Application Information

1. Typical Application

This section describes a 2.1 Master and Slave application. The Master (U1 AXS2050) is configured as stereo BTL outputs with 400-kHz switching frequency and no power limit implemented, and the Slave (U2) is configured as a mono PBTL output. Both U1 and U2 are setup with a gain of 26-dB. Inputs are connected for differential inputs.

32. AXS2050 in a 2.1 Mode Application

2. Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range PVCC	5 V to 26 V
PWM output frequencies	300kHz, 400 kHz, 500 kHz, 600 kHz, 1 MHz or 1.2 MHz
Maximum output power	2 × 70 W

3. Detailed Design Procedure

The AXS2050 devices are very flexible and easy-to-use Class D amplifiers; therefore, the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

PVCC rail planned for the design

Speaker or load impedance

Maximum output power requirement

Desired PWM frequency

3.1 Select the PWM Frequency

Set the PWM frequency by using AM0, AM1 and AM2 pins.

3.2 Select the Amplifier Gain and Master/Slave Mode

To select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that corresponds to produce an output voltage swing greater than the required output swing for maximum power. The analog gain and master/slave mode can be set by selecting the voltage divider resistors (R1 and R2) on the Gain/SLV pin.

3.3 Select Input Capacitance

Select the bulk capacitors at the PVCC inputs for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed power supply, two 100- F, 50-V capacitors should be sufficient. One capacitor should be placed near the PVCC inputs at each side of the device. PVCC capacitors should be a low ESR type because they are being used in a fast-switching application.

3.4 Select Decoupling Capacitors

Good quality decoupling capacitors must be added at each of the PVCC inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances.

3.5 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22- F, 25-V capacitors of X5R quality or better.

4. Power Supply Recommendations

The AXS2050 device requires an external power supply, between 4.5 V and 26 V, for the analog circuitry (AVCC) and the power stage (PVCC) of the amplifier. Several on-chip regulators are included on the AXS2050 to generate the voltages necessary for the internal circuitry of the audio path. The voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The AVCC supply feeds internal LDO including GVDD. This LDO output are connected to external pins for filtering purposes, but should not be connected to external circuits. GVDD LDO output have been sized to provide current necessary for internal functions but not for external loading.

4.1 Power Supply Mode

The AXS2050 supports both single and dual power supply modes. For dual power supply mode application, when AVCC is supplied with 4.5-V power, PVCC is recommended to be lower than 20 V. When PVCC is supplied with power greater than 20 V, AVCC is recommended to be higher than 6 V.

4.2 Layout Guidelines

The AXS2050 can be used with a small, inexpensive ferrite bead output filter in most applications. However, because the Class-D switching edges are fast, the layout of the printed circuit board must be planned carefully. The following suggestions helps to meet EMC requirements.

Decoupling capacitors The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220- F or greater) bulk power supply decoupling capacitors should be placed near the AXS2050 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220-pF and 1-nF, and a larger mid-frequency cap of value between 100-nF and 1-µF also of good quality to the PVCC connections at each end of the chip.

Minimize the current loop from each of the outputs through the ferrite bead filter and back to GND. The size of this current loop determines its effectiveness as an antenna.

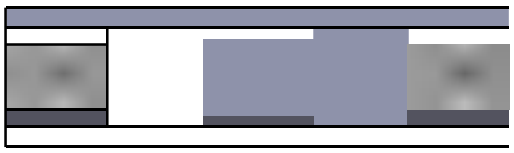
Grounding The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the AXS2050.

Output filter The ferrite EMI filter (see 29) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

5. Layout Example

图33. Layout

6. Heat Sink Used on the EVM



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