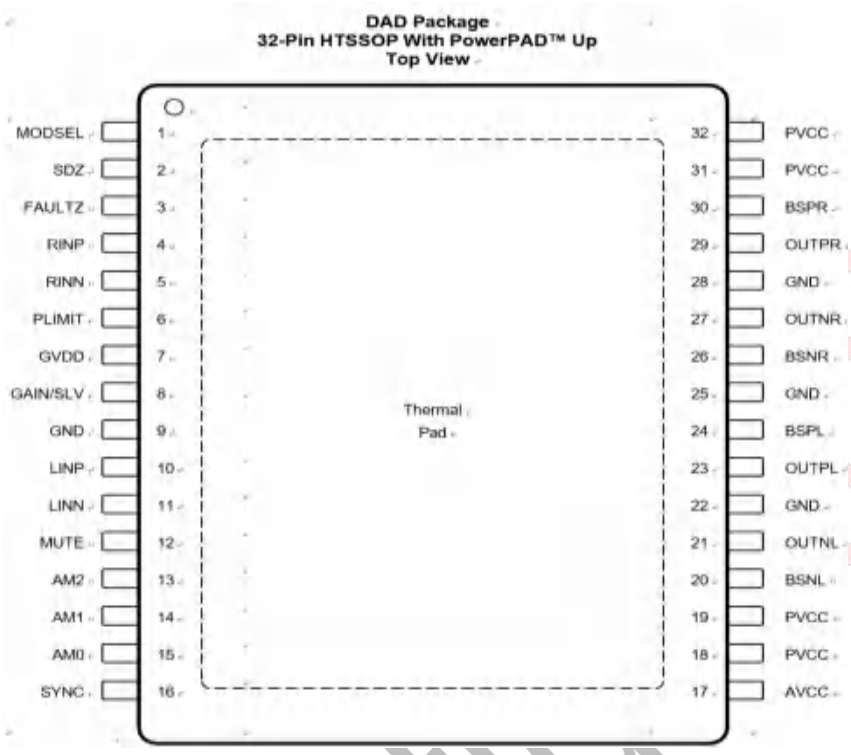
Description

The AXS2050 is a 2 x 50W high-efficiency stereo, low-idle-current Class-D amplifier in a thermally enha56 8250W

Pin Configuration and Functions



PIN	TYPE(1)

20	BSNL	BST	Boot strap for negative left channel output, connect to 220 nF X5R, or better ceramic cap to OUTPL
21	OUTNL	PO	Negative left channel output
23	OUTPL	PO	Positive left channel output
24	BSPL	BST	Boot strap for positive left channel output, connect to 220 nF X5R, or better ceramic cap to OUTNL Refer to: BSPx and BSNx Capacitors
22, 28	GND	G	Ground
26	BSNR	BST	Boot strap for negative right channel output, connect to 220 nF X5R, or better ceramic cap to OUTNR. Refer to: BSPx and BSNx Capacitors
27	OUTNR	PO	Negative right channel output
29	OUTPR	PO	Positive right channel output
30	BSPR	BST	Boot strap for positive right channel output, connect to 220 nF X5R or better ceramic cap to OUTPR. Refer to: BSPx and BSNx Capacitors
31, 32	PVCC	P	Power supply
		G	Connect to GND for best system performance. If not connected to GND, leave floating.

Order Information

Part Number	Package Type	Marking	Package Qty	Temp Range (°C)
AXS2050	HTSSOP32	AXS2050 XXXXXX XXXX	Tape and Reel, 2000	-40 to 125

ESD CAUTION: These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Specifications

1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	0.3	30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	0.3	6.3	V
	PLIMIT, GAIN/SLV, SYNC	0.3	GVDD+0.3	V
	AM0, AM1, AM2, MUTE, SDZ, MODSEL	0.3	PVCC+0.3	V
Slew rate, maximum(2)	AM0, AM1, AM2, MUTE, SDZ, MODSEL		10	V/ms
Operating free-air temperature, T_A		40	125	°C
Operating junction temperature , T_J		40	150	°C
Storage temperature, T_{stg}		40	125	°C
Lead Temperature (Soldering, 10s)			260	°C

(1) Stresses beyond th

3. Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}	5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL	2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 k , PV_{CC} = 26 V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ, MODSEL (V_I = 2 V, V_{CC} = 18 V)			50	μA
R_L(BTL)	Minimum load Impedance	Output filter: L = 10 μH, C = 680 nF	3.2	4		
R_L(PBTL)		Output filter: L = 10 μH, C = 1 μF	1.6	2		
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition	1			μH

4. Thermal Information

THERMAL METRIC		AXS2050 DAD(1) 32 PINS	UNIT
R_{JA}	Junction-to-ambient thermal resistance	N/A	°C/W
$R_{JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
$_{JT}$	Junction-to-top characterization parameter	1.2	°C/W
$_{JB}$	Junction-to-board characterization parameter	21	°C/W

For the PCB layout, see the AXS2050EVM user guide.

5. DC Electrical Characteristics

T_A = 25℃, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 , f_s = 400 kHz, hybrid mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V		1.5	5	mV

6. AC Electrical Characteristics

T_A = 25℃, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 26 dB, Inputs AC-coupled to GND		70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz,				

7. Typical Characteristics

f_s = 400 kHz (unless otherwise noted)

Typical Characteristics (continued)

f_s = 400 kHz (unless otherwise noted)

Typical Characteristics (continued)

f_s = 400 kHz (unless otherwise noted)

Detailed Description

1. Overview

The AXS2050 device is a highly efficient Class D audio amplifier with integrated 80m Ohms MOSFET. The device supports both stereo and mono BTL modes, as well as mono PBTL mode.

The AXS2050 may be configured for either master or slave operation by using the SYNC pin. This configuration helps prevent the audible beats noise.

2. Functional Block Diagram

3. Feature Description

3.1 Gain Setting and Master and Slave

The gain of the AXS2050 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four states set the GAIN in Master mode with gains of 20, 26, 32, and 36 dB respectively, while the next four states set the GAIN in Slave mode with gains of 20, 26, 32, and 36 dB respectively. The gain setting is latched during power- up and cannot be changed while the device is powered on.

Table 1 lists the recommended resistor values for different state settings.

Table 1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 k	OPEN	60 k
Master	26 dB	20 k	100 k	30 k
Master	32 dB	39 k	100 k	15 k
Master	36 dB	47 k	75 k	9 k
Slave	20 dB	51 k	51 k	60 k
Slave	26 dB	75 k	47 k	30 k
Slave	32 dB	100 k	39 k	15 k
Slave	36 dB	100 k	16 k	9 k

(1) Resistor tolerance should be 5% or better.

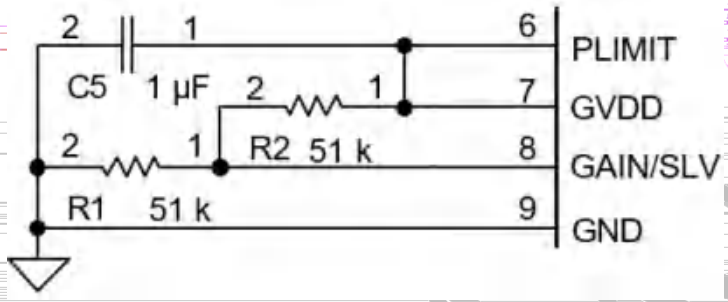


Figure 25. Gain, Master/Slave

In Master mode, the SYNC terminal is an output, while in Slave mode, the SYNC terminal is an input for a clock. TTL logic levels with compliance to GVDD.

3.2 Input Impedance

The AXS2050 input stage is a fully differential input stage and the input impedance changes with the gain Table 1 lists the values from min to max gain.

The tolerance of the input resistor value is ±20% so that the minimum value will be higher than 5.9 The inputs must be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF.

The input AC-coupling capacitor along with the input impedance forms a high-pass filter with the following cut-off frequency:

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. Table 2 lists the recommended AC-coupling capacitors for each gain setting. If a 3-dB frequency response is accepted at 20 Hz, 10 times lower capacitors (for example, a 1-µF capacitor) can be used.

Table2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	50 k	1.5 µF	2.1 Hz
26 dB	25 k	3.3 µF	1.9 Hz
32 dB	12.5 k	5.6 µF	2.3 Hz
36 dB	7.3 k	10 µF	2.2 Hz

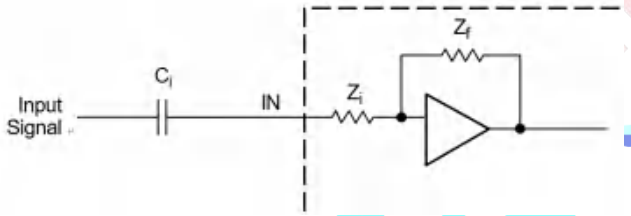


Figure 26. Input Impedance

The input capacitors should be a type of low leakage, such as quality electrolytic, tantalum, or ceramic caacitors.

If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

3.3 Startup and Shutdown Operation

The AXS2050 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for power conservation. The SDZ input terminal should be held high (see specification table for trip point)table for trip

Figure 27. Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This is done by limiting the duty cycle to a fixed maximum value. The limit can be considered as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately four times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$ for unclipped power

where

P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)

R_L is the load resistance.

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.

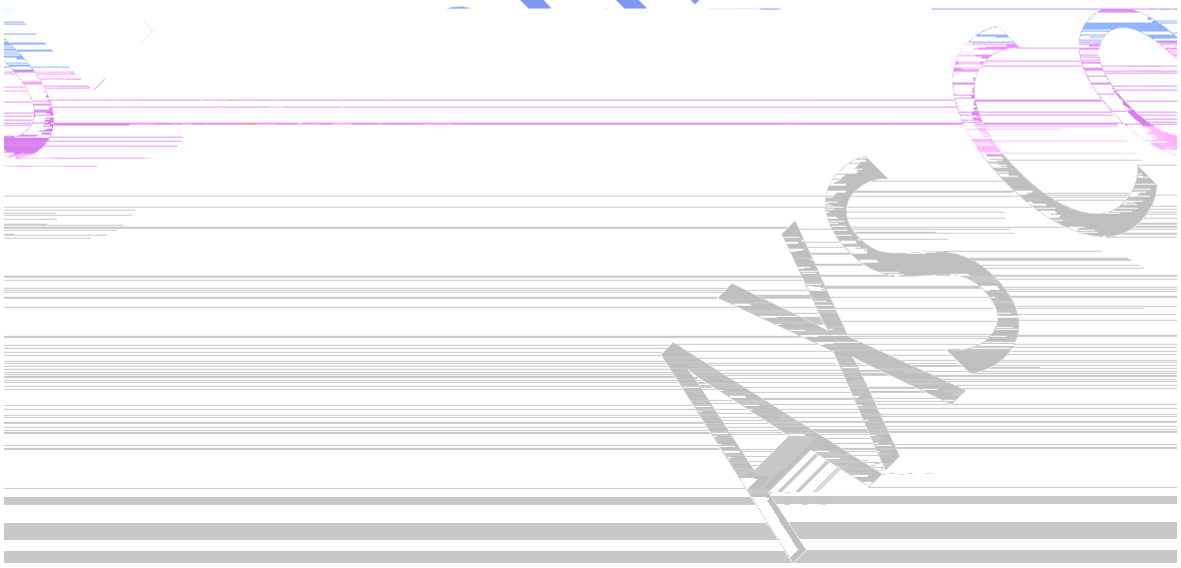
V_P is the peak amplitude, which is limited by the "virtual" voltage rail.

Table 3. Power Limit Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Open	Short	17.9
24 V	3.3	45 k	51 k	12.67

3.6 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-



3.9 DC Detect Protection

The AXS2050 has circuitry which protects the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault is reported on the FAULT pin as a low state. The DC Detect fault causes the amplifier to shutdown by changing the state of the outputs to Hi-Z.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC Detect protection latch. A DC Detect Fault is issued when the output differential voltage of either channel exceeds DC protection threshold level for more than 640 ms at the same polarity.

Table 5 shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. The Detect Protection Threshold feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Table 5 lists the minimum output offset voltages required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 640 ms to trigger the DC detect.

Table 5. DC Detect Threshold

PV_{CC} (V)	V_{OS} - OUTPUT OFFSET VOLTAGE (V)
4.5	1.35
6	1.8
12	3.6
18	5.4

3.10 Short-Circuit Protection and Automatic Recovery Feature

The AXS2050 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state. If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

3.11 Thermal Protection

Thermal protection on the AXS2050 prevents damage to the device when the internal die temperature exceeds 150°C. This trip point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault. Thermal protection faults are reported on the FAULTZ terminal as a low state.If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

4. Device Modulation Scheme

The AXS2050 is internally fixed to BD mode for better performance.

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires.

Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker.

The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages.

The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

Figure 28. BD Mode Modulation

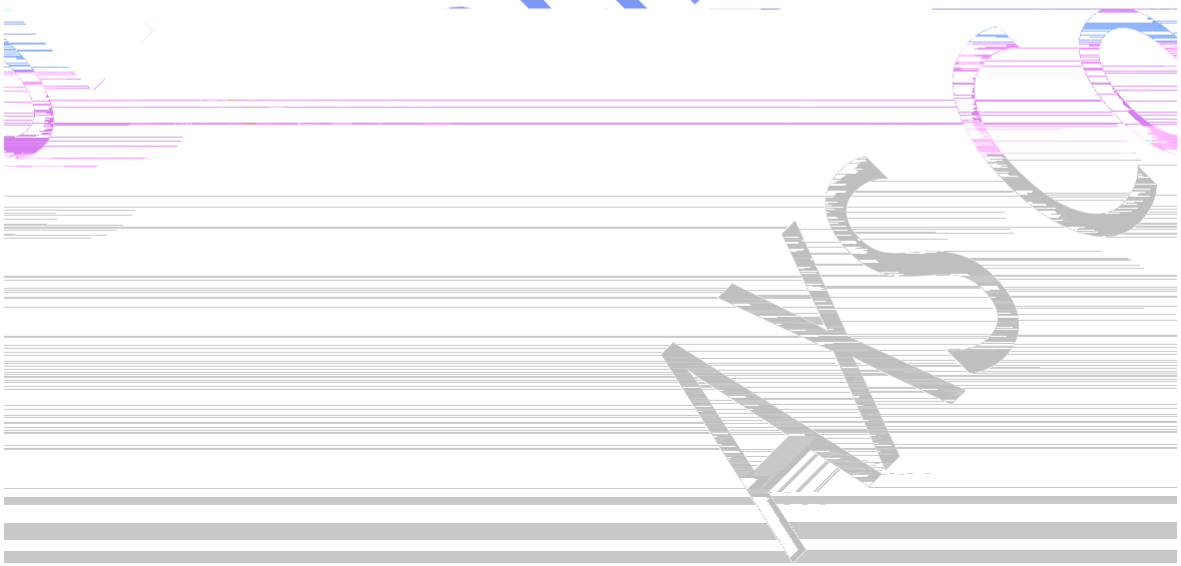
5. Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

Many traditional Class-D amplifiers are based on the AD modulation. Due to the out-of-phase nature of a BTL or PBTL amplifier operating in the AD modulation, if no LC filter was present, the load sees the full PWM signal across its terminals. This causes a high-frequency ripple current to pass through the load, which leads to high power dissipation, poor efficiency, and potential speaker damage. The ripple current is large in the AD modulation scheme, because it is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × VCC, and the time at each voltage is half the period for the AD modulation scheme. An ideal LC filter is required to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The modulation schemes implemented in the AXS2050 have little loss in the load even without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases and the pulses widen, the ripple current can go up. In this case, the ripple current can be filtered with an LC filter for increased efficiency. However, in most applications the filter is not required.

With an LC filter, specifically as the cut-off frequency of the LC filter is smaller than the PWM switching frequency of the amplifier, the ripple current is reduced such that only a small residual ripple voltage is present after the LC filter. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, hence increasing efficiency.

6. Ferrite Bead Filter Considerations



7. When to Use an Output Filter for EMI Suppression

A complete LC reconstruction filter should be added in some circuit instances. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in Figure 29 can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest-cost methods to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective in preventing line conducted interference.

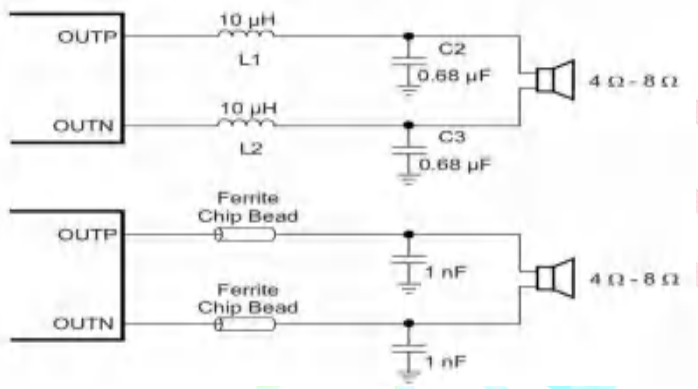


Figure 29. Output Filters

8. AM Avoidance EMI Reduction

Table 6. AM Frequencies

US AM FREQUENCY (kHz)	EUROPEAN AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
540-917	540-914	500	0	0	1
917-1125	914-1122	600 (or 400)	0	1	0
			0	0	0
1125-1375	1122-1373	500	0	0	1
1375-1547	1373-1548	600 (or 400)	0	1	0
			0	0	0
1547-1700	1548-1701	600 (or 500)	0	1	0
			0	0	1

9. Device Functional Modes

AXS2050 can be configured in either a stereo BTL (Bridge Tied Load) mode, mono BTL mode (only one output BTL channel active), or in a mono PBTL (Parallel Bridge Tied Load) mode.

9.1 Mono PBTL Mode

In mono PBTL mode, the device can deliver up to 100-W output power. Configuration steps for mono PBTL mode are as follows:

Connect LINP and LINN directly to Ground (without capacitors), so the device is set in a mono PBTL mode during power up.

Connect OUTPR and OUTNR together for the positive speaker terminal, and OUTNL and OUTPL together for the negative speaker terminal.

Analog input signal is applied to RINP and RINN.

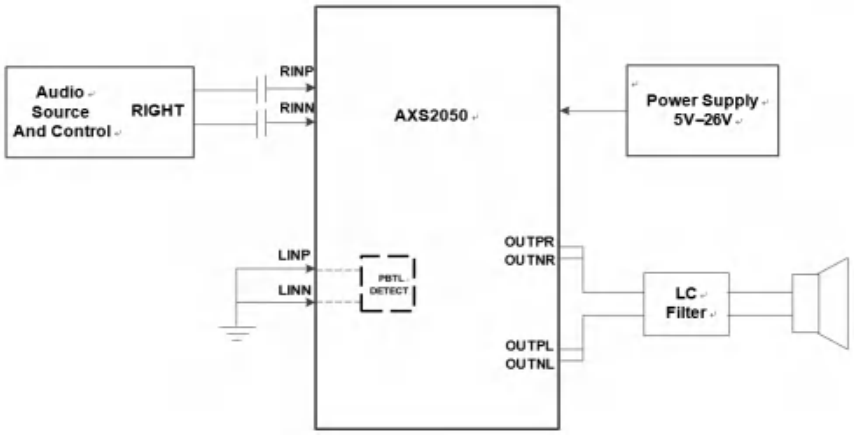


Figure 30. Mono PBTL Mode

9.2 Mono BTL

Mode (Single Channel Mode)

The AXS2050 can be connected in mono BTL mode while cutting the idle power-loss nearly by half.

Connect RINP and RINN directly to Ground (without capacitors), so the device is set in mono BTL mode during power up.

Connect OUTPL to the positive speaker terminal, and OUTNL to the negative speaker terminal.

Analog input signal is applied to LINP and LINN.

Figure 31. Mono BTL Mode

Application Information

1. Typical Application

This section describes a 2.1 Master and Slave application. The Master (U1 AXS2050) is configured as stereo BTL outputs with 400-kHz switching frequency and no power limit implemented, and the Slave (U2) is configured as a mono PBTL output. Both U1 and U2 are setup with a gain of 26-dB. Inputs are connected for differential inputs.

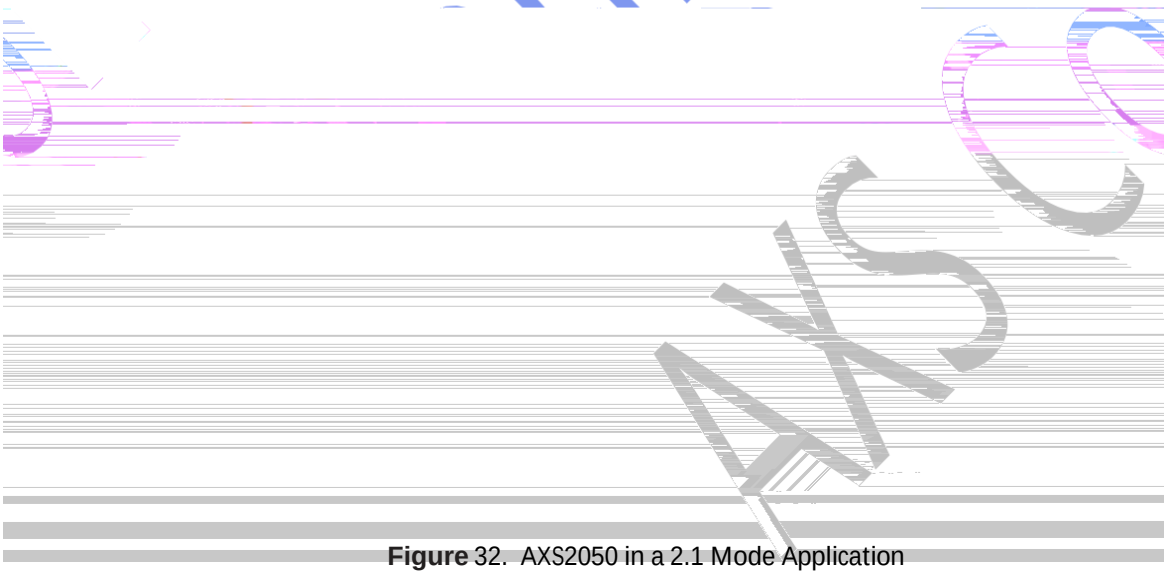


Figure 32. AXS2050 in a 2.1 Mode Application

2. Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range PVCC	5 V to 26 V
PWM output frequencies	300kHz, 400 kHz, 500 kHz, 600 kHz, 1 MHz or 1.2 MHz
Maximum output power	2 × 70 W

3. Detailed Design Procedure

The AXS2050 devices are very flexible and easy-to-use Class D amplifiers; therefore, the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

PVCC rail planned for the design

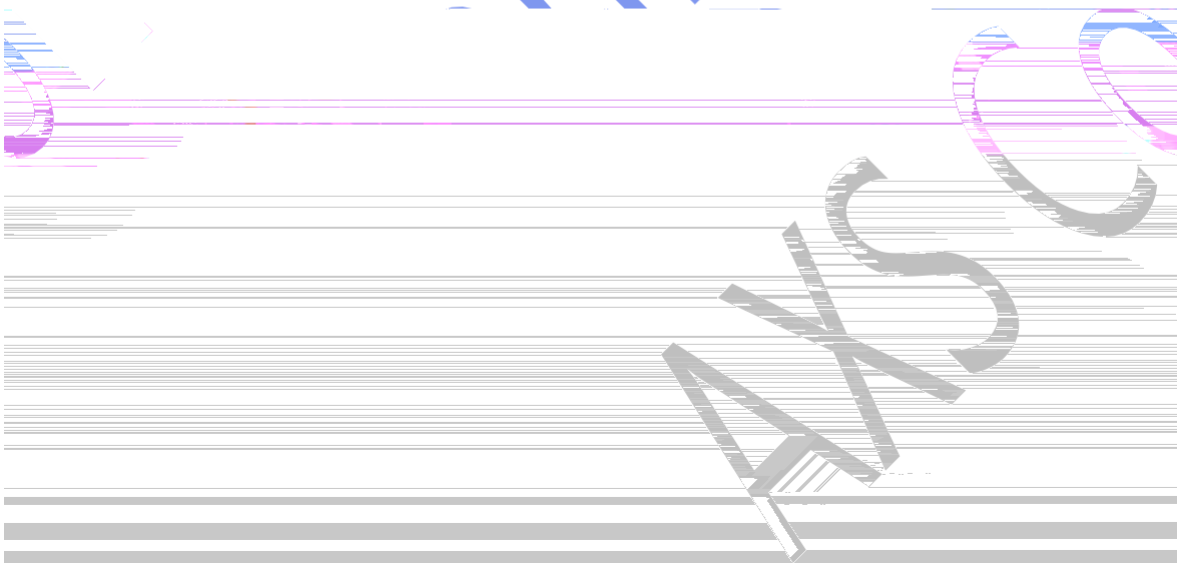
Speaker or load impedance

Maximum output power requirement

Desired PWM frequency

3.1 Select the PWM Frequency

Set the PWM



4. Power Supply Recommendations

The AXS2050 device requires an external power supply, between 4.5 V and 26 V, for the analog circuitry (AVCC) and the power stage (PVCC) of the amplifier. Several on-chip regulators are included on the AXS2050 to generate the voltages necessary for the internal circuitry of the audio path. The voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The AVCC supply feeds internal LDO including GVDD. This LDO output are connected to external pins for filtering purposes, but should not be connected to external circuits. GVDD LDO output have been sized to provide current necessary for internal functions but not for external loading.

4.1 Power Supply Mode

The AXS2050 supports both single and dual power supply modes. For dual power supply mode application, when AVCC is supplied with 4.5-V power, PVCC is recommended to be lower than 20 V. When PVCC is supplied with power greater than 20 V, AVCC is recommended to be higher than 6 V.

4.2 Layout Guidelines

The AXS2050 can be used with a small, inexpensive ferrite bead output filter in most applications. However, because the Class-D switching edges are fast, the layout of the printed circuit board must be planned carefully. The following suggestions helps to meet EMC requirements.

Decoupling capacitors The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220- F or greater) bulk power supply decoupling capacitors should be placed near the AXS2050 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220-pF and 1-nF, and a larger mid-frequency cap of value between 100-nF and 1-µF also of good quality to the PVCC connections at each end of the chip.

Minimize the current loop from each of the outputs through the ferrite bead filter and back to GND. The size of this current loop determines its effectiveness as an antenna.

Grounding The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the AXS2050.

Output filter The ferrite EMI filter (see Figure 29) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

5. Layout Example

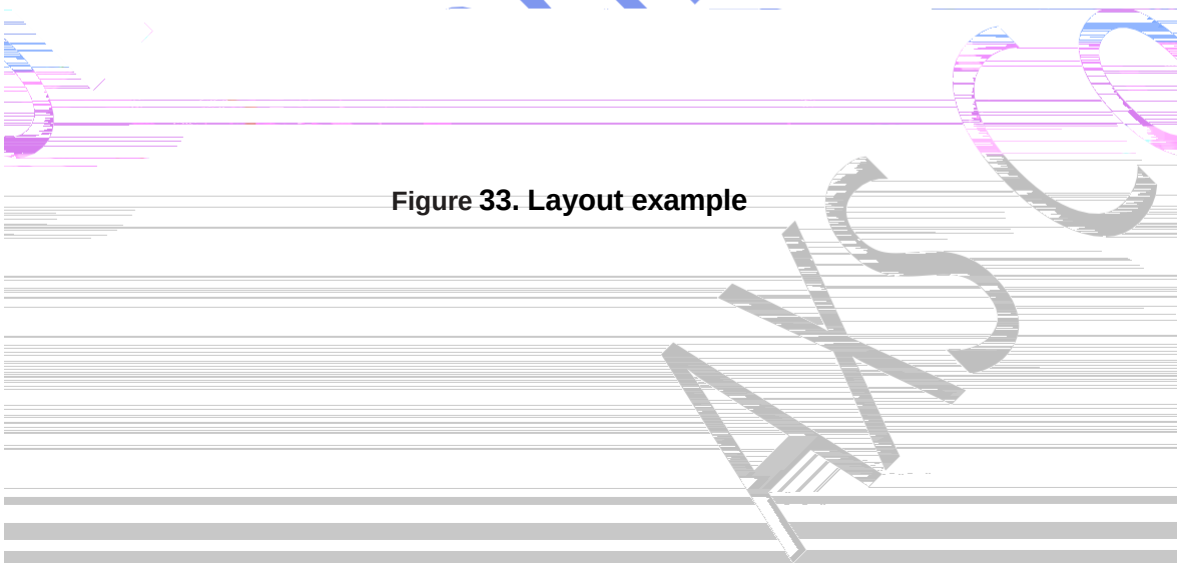
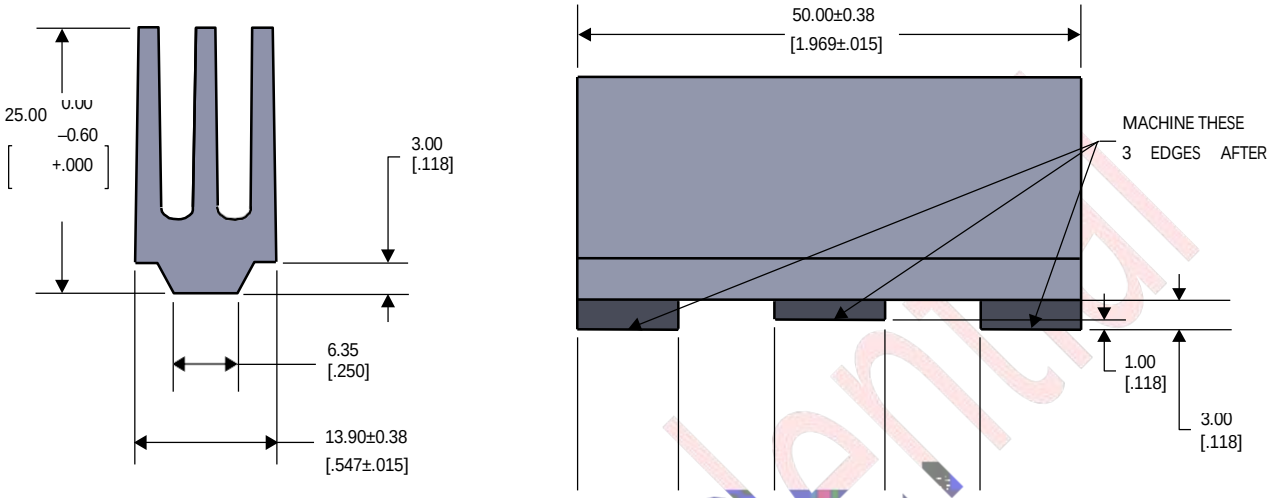
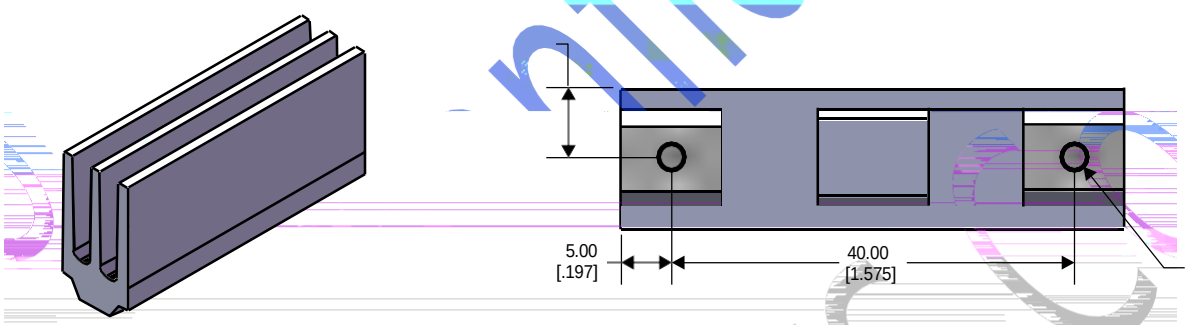


Figure 33. Layout example

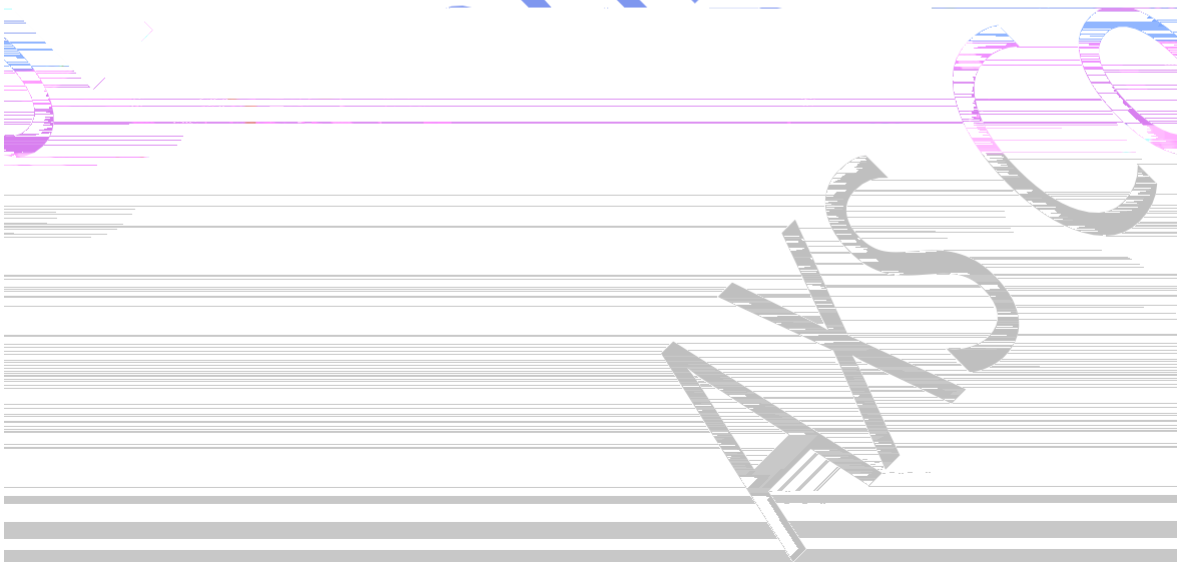
6. Heat Sink Used on the EVM

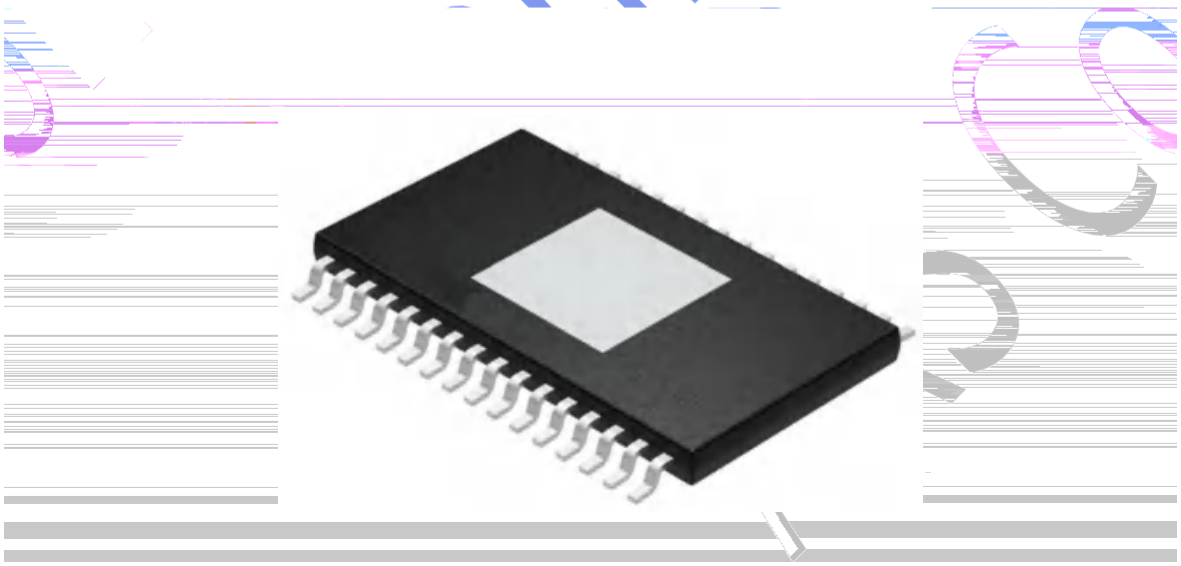
The heat sink (part number ATS-TI 10 OP-521-C1-R1) used on the EVM is an 14x25x50 mm extruded aluminum heat sink with three fins (see drawing below).





This size heat sink has shown to be sufficient for continuous





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